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FABRICATION AND MEASUREMENTS OF MEMORY DEVICES

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Abstract

Flash memory is nonvolatile memory (NVM) devices that do not need voltage to hold information or data. Nanostructures such as Silicon nanowires (SiNWs) are used as a medium for charge storage. In this laboratory experiment, SiNWs are grown, the plasma enhanced chemical vapour deposition (PECVD) process is used in the deposition of the SiNWs which is sandwich between the metal contact and the P-type substrate, and the deposition of 100nm thickness of silicon nitride is used as the insulator layer. The fabrication of the memory device will be performed in accordance with the laboratory experiment procedure, the current – voltage and capacitance with varying frequencies measurement will be carried out, and the characteristics behavior will be analyzed and discussed.

***Keywords**: Memory, Volatile, Non – volatile, Retention, Flash memory, Silicon Nanowires, Floating gate.*

INTRODUCTION

The electronics industry is fast transiting from the dominance by home electronics and appliances market to fast-rising mobile electronics market, most of the apparent examples of the electronic gadget which are filling the consumer's pockets are the handheld computers, cellular telephones and digital music players (Forni *et al*., 2008).

In microelectronics, the memory devices play more important role which is considered as the technology drivers; the electronic memory covers about 20%

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of semiconductor markets. The memory devices can be divided into two categories which are; the volatile memories and the non-volatile memories. The volatile memories such as Random Access Memory (RAM), Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) has very high write-erase operations but these type of memories losses data when the supply voltage is removed. The non – volatile (NVM) memories such as the Read Only Memory (ROM), Erasable Programmable Read Only Memory (EPROM, Electronically Erasable Programmable Read Only Memory (EEPROM) and the flash memory which retains its content when power is removed (Brewer, 2008) has very low write - erase speed that requires high voltage with long retention. The retention time is the length of time in between the stored data and the first invalid data that is read out, the typical retention time specification at present for NVM is 10 years (Saranti *et al*., 2016).

In the semiconductor industry, the NVM have significant attention (Li and Chen, 2009). The main objective for NVM technology is need for high storage density with reduced cell size, high performance, low-cost memory device (Brewer, 2008). Flash memory which is a type of NVM provides a low cost, high performance and has a retention time of about 10 years, the storage mechanisms in a flash represent data by holding charge in the floating gate (Li and Chen, 2009).

In this laboratory experiment, the aim and objectives are to fabricate and characterize electronically metal -insulator -semiconductor with low – power and high-performance NVM (flash memory) by using the silicon nanostructures to fabricate a charge – storing element from selected catalyst.

FABRICATION PROCESS OF METAL INSULATOR SEMICONDUCTOR (MIS) MEMORY DEVICE

A P-type silicon wafer with a thin native oxide of 1 – 2nm was used in the fabrication of the memory device. The cleaning of the silicon wafer was carried out to remove impurities from the surface of the substrate; the cleaning process was carried out with Decon 90 soap, Isopropanol and Deionized water (DI), each of the process was carried out for 15 minutes. Buffered HF was not used in the cleaning process because the native silicon oxide layer is needed in the fabrication process. The bottom contact was carried out by the use of thermal

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vacuum evaporator (Edwards – AUTO 306) to deposit 100 – 150nm Aluminium and annealing in Nitrogen (N_2) atmosphere at 500°C for 15 minutes to form an ohmic contact at the rough surface (back) of the P-type silicon wafer.

Metal nanoparticles were deposited on the polish surface of the silicon wafer by the use of thermal vacuum evaporation, followed by the deposition of silicon nitride (SiN_2) of 5nm to form the tunnelling layer which is an insulator. The deposition of Tin (Sn) seed/catalyst layer (poly/crystalline silicon) for the growing of SiNWs was carried out. The PECVD process was used in growing of SiNWs with deposition condition of: Hydrogen flow rate = 100 sccm, Silane flow rate = 20 sccm, Pressure = 500 mTorr, Temperature = 400ºC, RF power = 12Watts, Deposition time = 5 minutes. The deposition of Silicon Nitride was performed using Nitrogen flow rate = 100 sccm, Ammonia flow rate = 40 sccm, Silane flow rate = 6.6sccm, Pressure = 350 mTorr, Temperature = 300ºC, RF power = 20Watts, Growth time = 20 minutes.

The memory device was completed by the deposition of silicon nitride (SiN_2) (which is also an insulator) of 100nm where the thickness was measured by the use of polarized ellipsometer which uses light waves to measure the thickness and then followed by the deposition 100 – 150nm Aluminium to the top contact by evaporation under the vacuum evaporator.

The analysis of scanning electron microscopy (SEM) was performed to examine the spatial distribution of the SiNWs on the silicon substrate (Saranti et al., 2016). The electrical measurement for the fabricated memory devices was carried out to measure the relationship between current-voltage (I -V) to measure the leakage current, capacitance – time (C - T) to find out the retention behaviour of the device and capacitance-voltage (C - V) with varying frequencies to calculate the charge storage.

Silicon NANOWIRES (SiNWs)

The use of nanowires have been of great importance because of their promising applications in nanoelectronics in the next generation; they are used as mediums that allows charge transport. Nanowire is used in NVM such as the flash memory and the semiconductor-oxide-nitride-oxide-semiconductor (SONOS) devices because of its intrinsic scalability (Li *et al*., 2007).

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Silicon nanowires (SiNWs) performs reliable write/read/erase operations with a very large memory window and high ON and OFF current ratio of about 10^5 which is highly useful application in NVM (Li *et al*., 2007).
SiNWs were used in the fabrication and characterization of the two terminal flash memory device with deposition of silicon nitride (N_2) to form the tunnelling layer of 5nm. The PECVD process was used to grow the SiNWs that will be used to store charges in the memory device. Metal particle of Tin (Sn) is deposited on the P-type Si substrate as catalyst layer for growing the SiNWs. Figure 1 shows the SEM image of SiNWs of about 70 – 80nm in diameter and about 2.5µm in length. From figure 1 below it can be observed that the Sn layer particles are still visible (i.e. not all the Sn particles are consumed).

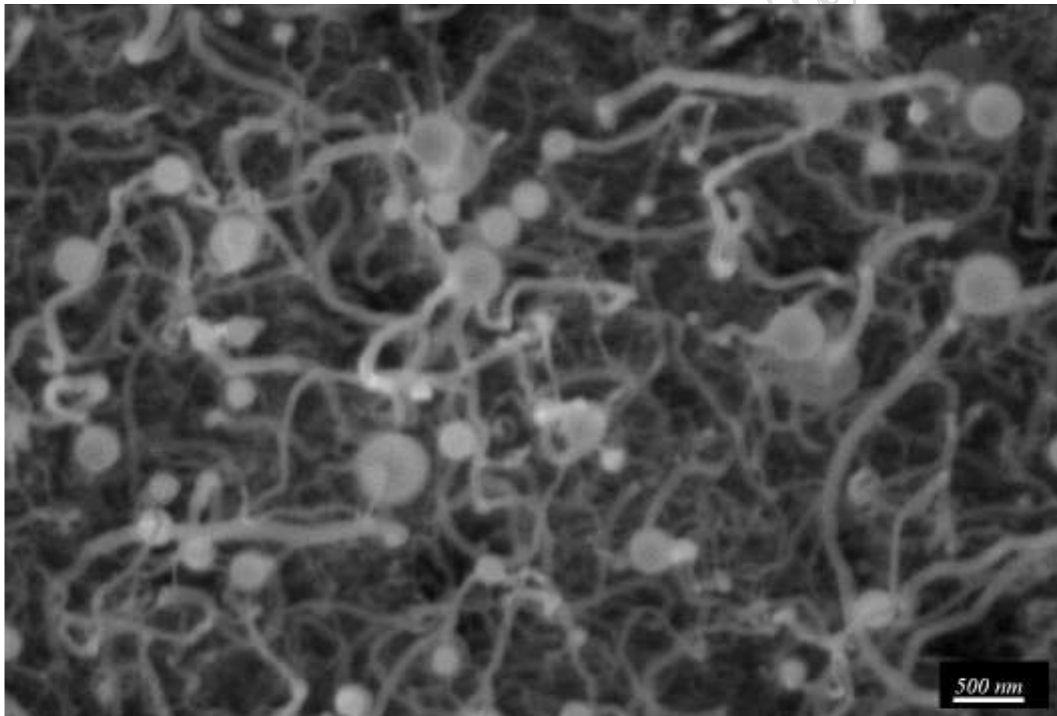

Fig.1: Morphology of Silicon Nanowires (SiNWs)

ELECTRICAL MEASUREMENT

Current-Voltage (I - V) Measurement

The I – V measurement was carried out to measure the leakage current and to confirm if the memory device was a good one, the leakage current measurement was obtained by using HP4140B pico – Ammeter. Voltage was applied in both

forward and reverse biased to the fabricated device, and the current flowing across the device was measured. If the leakage current obtained is in pico Ampere (pA), the device is a good one, the device is defective if otherwise, it implies that the device allows leakage current to flow.
Forward and reverse voltage of -3V to 3V and -5V to 5V respectively was applied to the memory device and the I – V measurement is shown in figure 2.

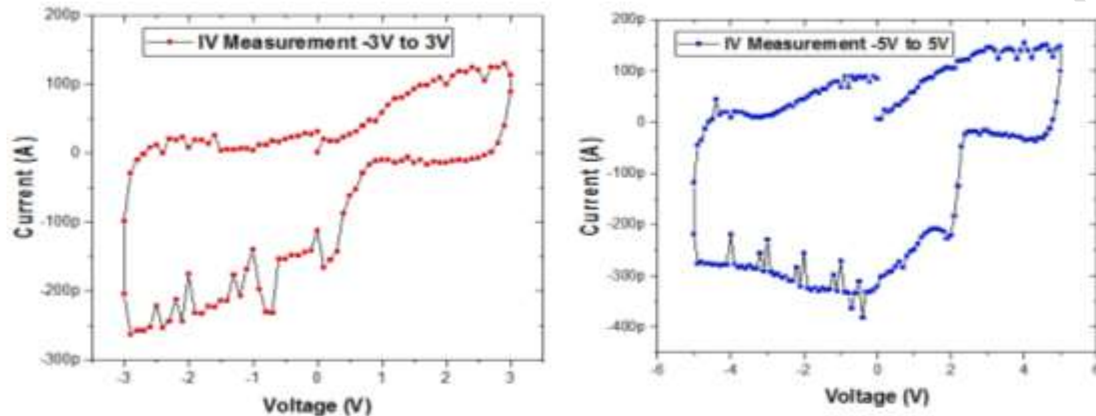

Fig.2: I - V Characteristics at voltage -3V to 3V and -5V to 5V

From figure 2, the hysteresis in the plot of the I – V characteristics implies that there is current drop and the electrons are not able to return through the same path, it also shows that the device is capable of storing charges (Saranti *et al*., 2016). From the I – V characteristics at 3V and 5V, it was observed that the leakage current of 100pA at 3V and 150pA at 5V was observed. The values of the leakage current gotten which is in pA shows that the fabricated device is a good one.

Capacitance-Voltage (C - V) Measurement with varying Frequency
In the C – V measurement, AC was applied with varying frequencies and Vrms of 0.150V, the measurement was performed by using HP4192A impedance analyser in a Faraday cage in other to avoid electromagnetic interference with the electrical measurement. For the P-type Metal insulator semiconductor (MIS), the applied voltage was changed by applying the bias in the inversion and accumulation region (Meena *et al*., 2014).
Figure 3 shows the C – V characteristics for the memory devices, Figure 4 shows the area enclosed by the C -V characteristics for the memory device at

different frequencies, and figure 5 shows the plot of the area calculated for the C – V characteristics against the varying frequencies.

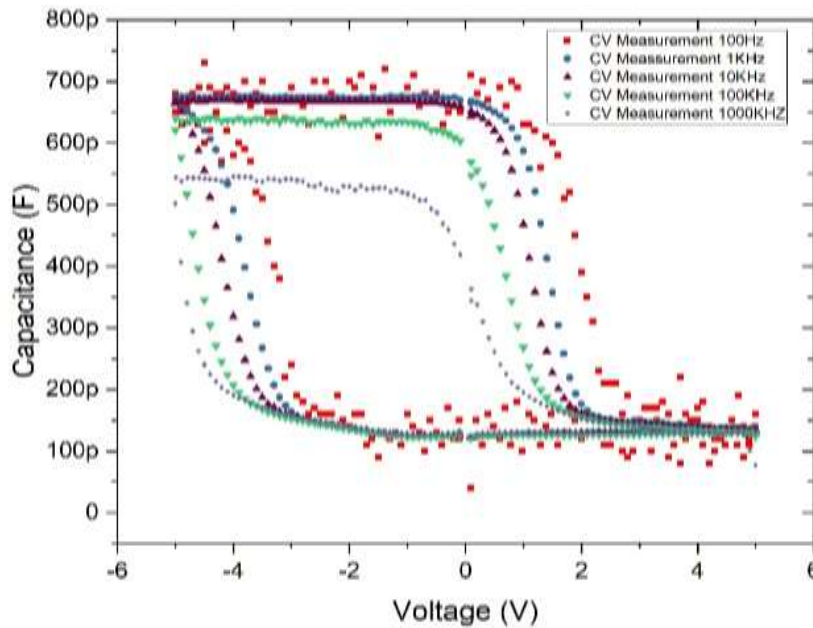

Fig. 3: C – V characteristics for memory devices with five (5) different frequencies

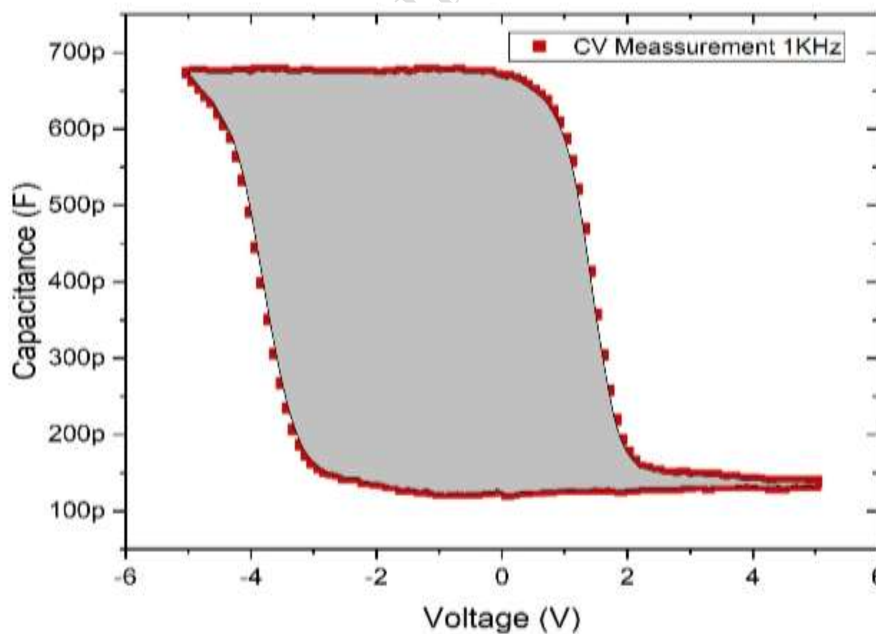

Fig. 4: The Plot of the Area enclosed by C – V Characteristics for the memory device for five frequencies

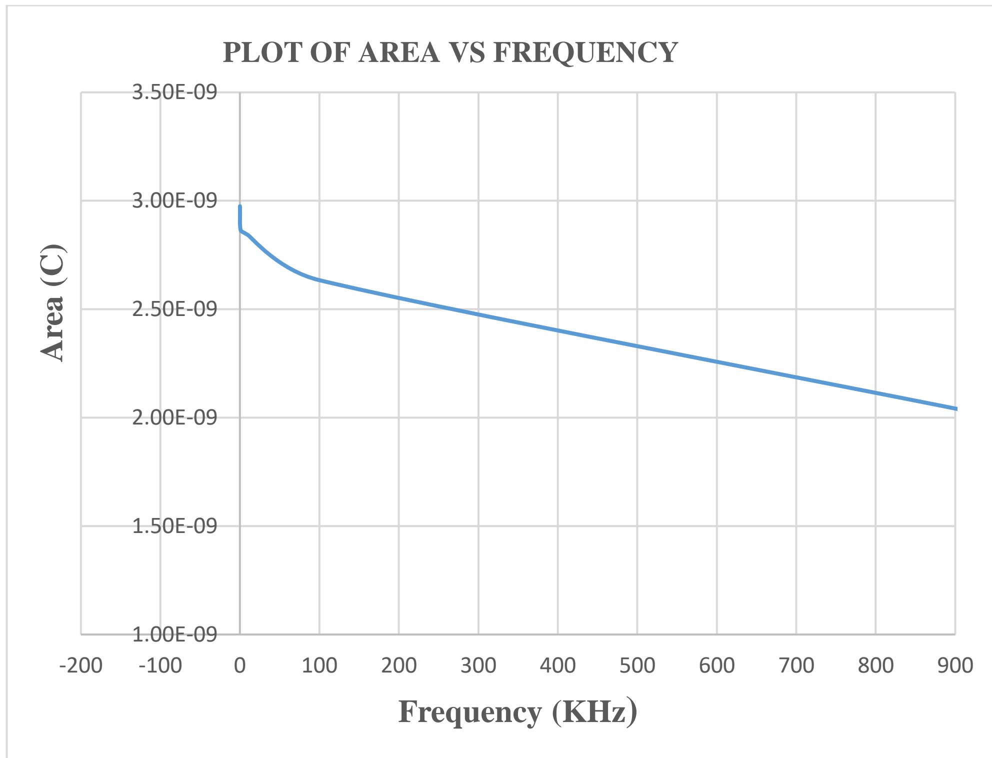

Fig. 5: Plot of Area Enclosed by C – V Characteristics against different frequencies

Fig.4 shows the plot of the area enclosed by C – V characteristics with frequency where the values for the area enclosed was calculated for 1KHz, the same procedure was carried out to calculate the values for area enclosed against different frequencies, and are summerised in table 1 below.

Table 1: The Area Enclosed by the C – V Characteristics of the memory device at different frequencies

Frequency (KHz)	Area (C)
0.1	2.9748×10^{-9}
1	2.8641×10^{-9}
10	2.84253×10^{-9}
100	2.6338×10^{-9}
1000	1.9689×10^{-9}

The hysteresis observed in the C – V characteristics in figure 3 shows the capability of charge storage by the SiNWs. From table 1 and figure 5, it can be

observed that, as the frequency increases, the area enclosed by the C – V characteristics decreases. This implies that at lower frequency, the area increases and more charges are stored because, the deep level defect found in the energy band gap of a semiconductor material can only respond to low values for C-V measurements (Saranti *et al.*, 2016), the low frequencies gives sufficient time for the majority carriers to get to the SiNWs where the charges are stored. The high - frequency capacitance does not provide deep level defects which makes the area enclosed in the C – V characteristics to become smaller and allows less amount of charges to be stored. From the plot, it can be concluded that there are differences in the area enclosed in the C – V characteristics for the fabricated memory device at different frequencies.

The calculated charge storage in the memory device is the values of the area enclosed in the C-V measurement for different frequencies. Since; $Q = C \times V$

Where;

Q = Charge store in the memory device (C)

Capacitance – Time (C – T) Measurement

The C – T characteristics gives the retention behaviour of the memory device. The write, read and erase voltage 5V, and a 0.1sec pulse was applied, and the capacitance was measured with time.

Figure 6 shows the C – T characteristics of the memory device.

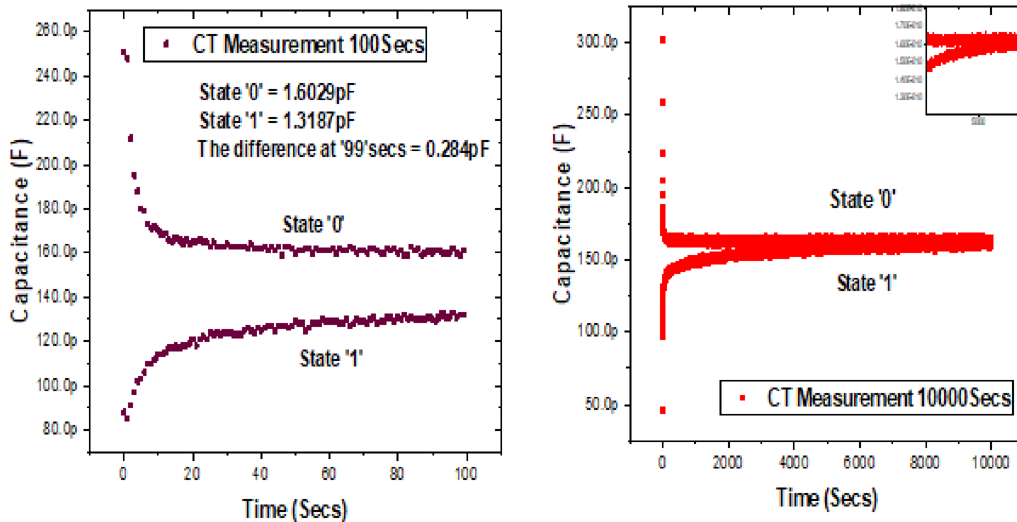

Fig. 6: C – T Characteristics to measure the retention time different time variations

For MIS devices it stores charges even as the applied voltage is removed (i.e. it has long retention time). Figure 6 shows the C-T characteristics to measure the retention time for the memory device. Two states which are state ‘0' and state ‘1' from the plot shows the data retention time of the memory device. State ‘0'with higher capacitance represents the write state of the memory device and state ‘1' with lower capacitance represents the erase state of the memory device. The maximum time in which the memory can store charges is not yet known; it will take the next 10 years for NVMs (Saranti *et al*., 2016). From the plot in figure 6, the C – T measurement for 100 secs shows that it is a good memory device because the write (0) state and the erase (1) state is distinctly shown not merge together, the differences is about 0.284pF which implies that the device has a longer retention capability. For the C – T characteristics for 10000 secs the write (0) state and the erase (1) state is merged together which implies that the device cannot retain data for a long time.

THE WORKING PRINCIPLE OF FLASH MEMORY DEVICE

The flash is NVM memory which does not need voltage supply to hold its information. It is an alternative memory that store charges, it is used widely in consumer electronic products such as the music players, cell phones, laptops, desktops etc.(Meena *et al*., 2014).

Nor and NAND flash is among the flash memories that have been designed which are proposed for the commercial market. For code and data storage application the operation speed of the NOR flash is high and which is also characterized by direct write and large cell size (i.e. in bytes) while the NAND is a page write and small cell size which has a high-density storage application for data (Meena *et al*., 2014).

The working principle of the flash memory is based on the floating gate (FG) component; the FG is between the gate and drain-source area of the MIS which is been isolated by an oxide layer. The gate can control the source-drain current if the FG is not charged, when a high voltage is applied to the gate the FG is been filled with electrons which creates a tunnel effect while the negative potentials on the FG work against the gate and does not allow current to pass through. Applying a high voltage in the reverse direction of the gate will erase

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the FG, the flash memory can retain information even as the power supply is turned OFF (Meena *et al*., 2014).

PROBLEMS WITH CURRENT FLASH MEMORY TECHNOLOGY

Low internal programming voltage: the size of the memory cell for a flash memory is limited due to the isolation of nodes in flash memory cells that are used for high programming voltages and scaling of storage of hot – carrier injection transistors, however, this may lead to the basic scaling limits since the minimum tunnel oxide thickness for 10 year retention to be achieved requires the programming of charge onto the FG by the use of high internal voltages (Derbenwick and Brewer, 2008).

Fast programming time: the dynamics of charge injection or removal of charge from the FG controls the write and erase speed of the flash memory device, this leads to slow programming speed of the device. The flash memory has a write speed of the order of 10µs to 2ms which is very slow as compares to the volatile memories that have write speed of 100ns (Derbenwick and Brewer, 2008).

Unlimited endurance: the endurance of the flash memory is affected by the intrinsic charging of the tunnel oxide and the tunnel oxide damages which is as a result of repeated injection of charges through them, the unlimited endurance of flash memory can also limit the reliability of the device due to the interrelationship between the endurance and the failure rate of the device (Derbenwick and Brewer, 2008).

Random erase: flash memory is limited by the effect of random erase, in flash memory, once a cell in the flash memory is damaged it affects the loss of information or data in the memory devices (Derbenwick and Brewer, 2008).

REMEDY FOR THE LIMITATIONS OF FLASH MEMORY

Silicon nanostructures such as SiNWs has the features for averting the limitations of the flash memory because they are used as a medium for storing charge or data, low cost, high performance and have long retention time (Saranti *et al*., 2016) than the conventional transistor memory. They are just two terminal devices with high mobility, high performance, consume less power and dissipate less heat (Meena *et al*., 2014). In the use of SiNWs, the information or

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data is not affected by the whole device even if a strand of wire of the nanostructure is damaged.

CONCLUSION

The laboratory experiment for the fabrication and electrical measurements of memory device was performed in accordance with the experimental procedures and the data that were given in the laboratory experiment. SiNWs were used as medium for stage of charges, the I – V characteristic behaviour shows a significant hysteresis that indicates that charges are stored, and the C – V characteristics with varying frequencies also shows the presence of charge storage in the SiNWs structure and how the area of the stored charges varies with frequency. The C – T characteristic behaviour gives the retention time for the fabricated memory device which shows the write and the erase state of the device.

From plot of the I -V, C -V and C -T characteristics behaviour, it shows that the fabricated device is capable to hold charge and retain charge as a memory device.

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